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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,846	02/20/2004	Yuen-Foo Michael Kou	09215-011001	7511

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EXAMINER	
HOLLINGTON, JERMELE M	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 02/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,846	MICHAEL KOU, YUEN-FOO	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Due to a mistake of the previous Office Action, the examiner below is providing an updated and correct Office Action.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-11, 15-28, and 30-37 are rejected under 35 U.S.C. 102(a) as being anticipated by Kou (20030030429A1).

Regarding claim 1, Kou discloses a method of assembling multiple electronic components (tray 326) to a circuit board (not shown but see paragraphs [0025] and [0027]), the method comprising: securing an electronic component (326) to the circuit board (see paragraphs [0025] and [0027]); creating an association between the secured electronic component (326) and an environmental condition recorder (environmental condition recorder 202) [see Fig. 3E]; recording data [via remote device 214] from the environmental condition recorder (202), the data indicating exposure of the secured electronic component (326) to an environmental condition over time (see paragraph [0023]); and determining [via remote device 214], based on the recorded data, whether the secured electronic component (326) is suitable for exposure to conditions associated with securing a second electronic component (326) to the circuit board.

Regarding claim 2, Kou discloses for said secured electronic component (326) found suitable, exposing the suitable secured electronic component (326) to conditions associated with securing said second electronic component (326) to the circuit board.

Regarding claim 3, Kou discloses maintaining the association between the secured electronic component (326) and the environmental condition recorder (202) from shortly after securing the electronic component (326) until determining suitability.

Regarding claim 4, Kou discloses the environmental condition recorder (202) is adapted to continually monitor and periodically record an ambient environmental condition.

Regarding claim 5, Kou discloses the environmental condition recorder (202) is adapted to automatically record an ambient environmental condition over time.

Regarding claim 6, Kou discloses the conditions associated with securing said second electronic component (326) to the circuit board comprise exposing the secured electronic component (326) to conditions associated with reflow soldering the second component (326) to the circuit board.

Regarding claim 7, Kou discloses the conditions associated with securing the second electronic component (326) to the circuit board comprises exposing the secured electronic component (326) to an elevated temperature (see paragraphs [0023] and [0027]).

Regarding claim 8, Kou discloses recording the data from the environmental condition recorder (202) comprises storing data [via memory device 210] that is indicative of the secured electronic component's (326) exposure to atmospheric moisture content (see paragraphs [0023] and [0044]).

Regarding claim 9, Kou discloses the data indicative of atmospheric moisture content comprises temperature measurements [via sensing element 204] and percent relative humidity measurements collected by the environmental condition recorder (202) over time (see paragraphs [0045]-[0050].

Regarding claim 10, Kou discloses [see Fig. 3E] creating the association between the secured electronic component (326) and the environmental condition recorder (202) comprises physically attaching the environmental condition recorder (202) to the circuit board (not shown).

Regarding claim 11, Kou discloses creating the association between the secured electronic component (326) and the environmental condition recorder (202) comprises creating a logical association between the secured electronic component (326) and the environmental condition recorder (202) in a computer database (remote device 214).

Regarding claim 15, Kou discloses recording the data from the environmental condition recorder (202) comprises recording the data to a memory storage unit (memory storage unit 210) within the environmental recorder (202).

Regarding claim 16, Kou discloses accessing the recorded data from the memory storage unit (210), for the suitability determination over a communication channel.

Regarding claim 17, Kou discloses recording data from the environmental condition recorder (202) comprises recording data to a memory storage unit (222) that is located external to the environmental condition recorder (202).

Regarding claim 18, Kou discloses estimating a cumulative effect that exposure to the recorded environmental conditions would have on the secured component.

Regarding claim 19, Kou discloses estimating the cumulative effect that exposure to the recorded environmental conditions would have approximates integrating effects of exposure to the recorded environmental conditions over time.

Regarding claim 20, Kou discloses estimating the cumulative effect that exposure to the recorded environmental conditions would have comprises referencing industry standard guidelines related to expected total floor life for the secured electronic component (326) under particular environmental conditions.

Regarding claim 21, Kou discloses [see Fig. 2] the environmental condition recorder (202) comprises: a sensing element (204) responsive to an environmental condition, a memory storage unit (memory unit 210) in electronic communication with the sensing element (204) and adapted to store environmental condition data sensed by the sensing element (204); and a processing unit (processor 208) in electronic communication with the sensing element (204) and the memory storage unit (210).

Regarding claim 22, Kou discloses the processing unit (208) is adapted to record the data from the environmental condition recorder (202) by periodically sampling the sensing element (204) and electronically storing the sample in the memory storage unit (210).

Regarding claim 23, Kou discloses the processing unit (208) is adapted to determine whether the secured component (326) is suitable for exposure to conditions associated with securing said second electronic component (326) to the circuit board by evaluating the sample, stored in the memory storage unit (210).

Regarding claims 24-25, Kou discloses a method of securing multiple sets of electronic components (tray 326) to a circuit board (not shown but see paragraph [0025] and [0027]), the

method comprising: reflow soldering a first set of electronic components (326) to said circuit board; creating an association between the first set of electronic components (326) and an environmental condition recorder (202); collecting environmental exposure data with the environmental condition recorder (202), the environmental exposure data being associated with the first set of electronic components (326); storing [via memory device 210] the collected data in the environmental condition recorder (202), estimating, with the environmental condition recorder (202), a cumulative effect of the environmental exposure on each electronic component (326) of the first set, based on the stored data; and evaluating, with the environmental condition recorder (202), whether each electronic component (326) of the first set is suitable for exposure to environmental conditions associated with reflow soldering the second set of electronic components (326) to the circuit board.

Regarding claim 26, Kou discloses the conditions associated with reflow soldering set of electronic components (326) to the circuit board comprise an elevated temperature.

Regarding claim 27, Kou discloses collecting environmental exposure data comprises collecting temperature measurements [via sensing element 204] and relative humidity measurements.

Regarding claim 28, Kou discloses the association comprises attaching the environmental condition recorder (202) to the circuit board.

Regarding claim 30, Kou discloses storing the collected data comprises storing the collected data in a memory storage unit (memory unit 210) within the environmental condition recorder (202).

Regarding claim 31, Kou discloses the collected data comprises temperature measurements [via sensing element 204] and relative humidity measurements collected over time and wherein estimating the cumulative effect of the environmental exposure comprises integrating the temperature measurements and relative humidity measurements with respect to time.

Regarding claim 32, Kou discloses evaluating whether each electronic component (326) of the first set is suitable for exposure to environmental conditions associated with reflow soldering the set of electronic components (326) to the circuit board comprises referencing industry standard guidelines.

Regarding claim 33, Kou discloses collecting the environmental exposure data associated with the first set of electronic components (326) comprises using said environmental condition recorder (202) to continually monitor and periodically and electronically record said environmental condition.

Regarding claim 34, Kou discloses collecting the environmental exposure data associated with the first set of electronic components (326) comprises using said environmental condition recorder (202) to automatically record environmental condition data.

Regarding claim 35, Kou discloses the environmental condition recorder (202) comprises: a sensing element (sensing unit 204) responsive to an environmental condition, a memory storage unit (memory unit 210) in electronic communication with the sensing element (204) and adapted to store environmental condition data sensed by the sensing element (204); and a processing unit (processor unit 208) in electronic communication with the sensing element (204) and the memory storage unit (210).

Regarding claim 36, Kou discloses the processing unit (208) is adapted to record the data from the environmental condition recorder (202) by periodically sampling the sensing element (204) and electronically storing the sample in the memory storage unit (210).

Regarding claim 37, Kou discloses the processing unit (208) is adapted to determine whether the secured component (326) is suitable for exposure to conditions associated with securing said second electronic component (326) to the circuit board by evaluating the sample, stored in the memory storage unit (210).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 12-14 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kou (20030030429) in view of Soga et al (5867809).

Regarding claim 12, Kou discloses a method of assembling multiple electronic components (tray 326) to a circuit board (not shown but see paragraphs [0025] and [0027]). However, he does not disclose circuit board comprising an identification code as claimed. Soga et al disclose an identification code (production number/date 12) is positioned on the circuit board (2), the identification code (12) providing sufficient information to enable identification of the secured component (27) and the circuit board (2) and wherein creating the association comprises logically linking, in a computer database, the secured electronic component (27) and the circuit board (2), based on information provided by scanning the identification code (12) [via

optical sensor 11]. Further, Soga et al teach that the addition of identification code on the circuit board is advantageous because it enables a sensor to identify the circuit board and its history data to determine if the circuit board is useable to the user. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Kou by adding identification code to the circuit board as taught by Soga et al in order to enable a sensor to identify the circuit board and its history data to determine if the circuit board is useable to the user.

Regarding claim 13, Soga et al disclose the identification code (12) positioned on the circuit board (2) is based on bar code technology.

Regarding claim 14, Soga et al disclose the identification code (12) is based on radio frequency technology.

Regarding claim 29, Kou discloses a method of assembling multiple electronic components (tray 326) to a circuit board (not shown but see paragraphs [0025] and [0027]). However, he does not disclose circuit board comprising an identification code as claimed. Soga et al disclose the association comprises scanning [via optical sensor 11] a bar code (production number/date 12) affixed to the circuit board (2), the bar code (12) identifying each electronic component (25 and 27) of the first set of components secured to the circuit board (2). Further, Soga et al teach that the addition of identification code on the circuit board is advantageous because it enables a sensor to identify the circuit board and its history data to determine if the circuit board is useable to the user. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Kou by adding identification code to the circuit board as taught by Soga et al in order to enable a sensor to

identify the circuit board and its history data to determine if the circuit board is useable to the user.

Conclusion

5. Applicant's arguments with respect to claims 1-37 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (517) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Primary Examiner
Art Unit 2829

JMH
January 24, 2006